

REMARKS

This amendment is being filed in response to the Office Action having a mailing date of May 2, 2005. Claims 1, and 8-10 are amended as shown. More particularly, independent claims 1, 8, and 9 are amended to recite certain distinctive subject matter. Claims 9-10 are amended to clarify that these claims do not fall within the scope of 35 U.S.C. § 112, sixth paragraph. New claims 11-14 have been added. No new matter has been added. With this amendment, claims 1-14 are pending in the application.

In the Office Action, the Examiner objected to claims 4-7 as being dependent upon a rejected base claim, but indicated that these claims would be allowable if rewritten in independent form to include the limitations of their base claims. The applicants thank the Examiner for the indication of allowable subject matter. New claims 11-14 are presented herein and recite distinctive subject matter, and are allowable. The requisite fee for these new claims is included herewith.

In the Office Action, the Examiner rejected claims 1-2 and 8-9 under 35 U.S.C. § 102(b) as being anticipated by Gupta (U.S. Patent No. 5,247,478). Claims 1, 3, and 8-10 were rejected under 35 U.S.C. § 102(e) as being anticipated by Sansbury (U.S. Patent No. 6,456,529). For the reasons that will be set forth below, the applicants kindly request the Examiner to reconsider and withdraw the rejections.

A disclosed embodiment will now be discussed in comparison to the applied references. Of course, the discussion of the disclosed embodiment, and the discussion of the differences between the disclosed embodiment and subject matter described in the applied references, do not define the scope or interpretation of any of the claims. Instead, such discussed differences are intended to merely help the Examiner appreciate important claim distinctions discussed thereafter.

One embodiment provides a non-volatile switch formed by a memory cell and a pass transistor. The memory cell and the pass transistor have a common floating gate region and a common control gate region. The result is a non-volatile cell with extremely reduced area. Moreover, it is possible to form the switch within a flash memory array, and hence providing increased compactness. In an embodiment, the memory cell and the pass transistor are integrated

adjacent to each other. *See, e.g.*, Figure 2 and the accompanying description the present application.

In still another embodiment, the switch is programmable switch. For example, the switch can block (or can pass) information supplied to the switch's input terminal to the switch's output terminal based on a programmable ON/OFF state. For instance, during the turning ON and OFF of the switch, the drain terminal FD is maintained floating, the source terminal FS is grounded, and digital data (binary 1 or 0) is supplied to the input of the pass transistor. *See, e.g.*, Figures 1 and 7 and the accompanying description in the present application.

Such features are not disclosed, taught, or suggested by any of the cited references. For example, Gupta fails to show any type of structure or layout such as those disclosed by the present applicants. Moreover, Gupta discloses a structure where the non-volatile cell belongs to a memory array (shown as a "memory plane" in Figures 2 and 4 of Gupta) that is formed in one part of the device, and the circuitry for the cited transistor is formed in a different part of the device (shown as a "logic plane" in Figures 2 and 4 of Gupta). The memory plane and the logic plane are in two different parts of the logic device of Gupta. *See, e.g.*, column 1, lines 53-65 of Gupta. Gupta is in sharp contrast to the embodiments disclosed in the applicants' specification, where the memory cell and the pass transistor are integrated adjacent to each other.

Sansbury relates to a programmable impedance device, and is not a pass transistor. More specifically, Sansbury does not disclose, teach, or suggest capability to program a switch in a manner that the switch can pass or block data supplied at to an input of the switch, based on a programmable ON/OFF state of the switch. Moreover, Sansbury does not disclose, teach, or suggest a memory cell and a pass transistor integrated adjacent to one another.

Accordingly, claim 1 has been amended to recite that the memory element and the pass transistor are integrated adjacent to each other. As explained above, this feature is not disclosed, taught, or suggested by any of the cited references. For instance, Gupta discloses a device where the memory cell and a cited transistor are formed in different parts of the device. Accordingly, amended claim 1 is now allowable.

Claim 1 is also made further allowable by now reciting that the switch is a programmable switch that can pass or block data from the input terminal to the output terminal based on programmable ON/OFF operation of the switch. There is no such feature to be found in or suggested by Gupta and/or Sansbury.

Claim 8 is amended to recite that the memory element and the pass transistor are integrated adjacent to each other. Claim 8 is amended to recite further allowable subject matter, namely, the device being a programmable switch that can pass or block data from the input terminal to the output terminal based on programmable ON/OFF operation of the switch. Because none of these features are found in or suggested by the cited references, amended claim 8 is now allowable.

Claim 9 is amended to recite that the memory element and pass transistor are integrated adjacent to each other. As explained above, this feature distinguishes over Gupta and/or Sansbury. Claim 9 is amended to additionally recite the distinctive feature --based on a programmable ON/OFF state of the switch, the datum is passed to an output terminal of the switch by the pass transistor or blocked from the output terminal of the switch by the pass transistor--. There is nothing in the cited references that involve a programmable switch with ON/OFF operation. Accordingly, amended claim 9 is now allowable.

Overall, none of the references singly or in any motivated combination disclose, teach, or suggest what is recited in the independent claims. Thus, given the above amendments and accompanying remarks, the independent claims are now in condition for allowance. The dependent claims that depend directly or indirectly on these independent claims are likewise allowable based on at least the same reasons and based on the recitations contained in each dependent claim.

If the undersigned attorney has overlooked a teaching in any of the cited references that is relevant to the allowability of the claims, the Examiner is requested to specifically point out where such teaching may be found. Further, if there are any informalities or questions that can be addressed via telephone, the Examiner is encouraged to contact the undersigned attorney at (206) 622-4900.

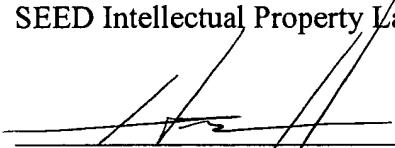
Application No. 10/760,637
Reply to Office Action dated May 2, 2005

The Director is authorized to charge any additional fees due by way of this Amendment, or credit any overpayment, to our Deposit Account No. 19-1090.

All of the claims remaining in the application are now clearly allowable. Favorable consideration and a Notice of Allowance are earnestly solicited.

Respectfully submitted,

SEED Intellectual Property Law Group PLLC



Harold H. Bennett II
Registration No. 52,404

DMD:wt

Enclosure:

Postcard

701 Fifth Avenue, Suite 6300
Seattle, Washington 98104-7092
Phone: (206) 622-4900
Fax: (206) 682-6031

588667_1.DOC